ABSTRACT OF THE DISCLOSURE

To provide a clock and data recovery circuit which facilitates alteration of the frequency range and adjustment of characteristics. The clock and data recovery circuit includes a phase shift circuit 101 having a switch receiving as inputs multi-phase clocks for selecting and outputting plural sets of the paired clocks from the input multi-phase clocks and a plural number of interpolators receiving the plural number of clock pairs output from the switch to output signals having the delay prescribed by the time corresponding to interior division of the phase difference of the clock pairs, a plural number of latch circuits 102 for latching the input data based on the signals output from the phase shift circuit 101, a counter 103 for counting the outputs of the plural latch circuits, a filter 105 for averaging the counter output over a preset time, a decoder 106 for decoding an output of the filter and a selection circuit 104 fed with a plural number of sets of data output by the plural latch circuits and clocks output from a preset one of the plural interpolators to select pairs of output data and clocks.